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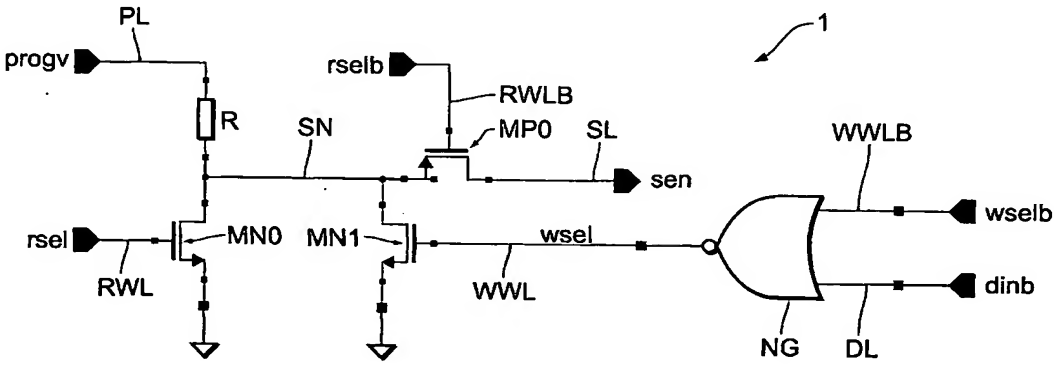
(54) Title: PROGRAMMABLE NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE



(57) Abstract: The present invention relates to a programmable non-volatile semiconductor memory device comprising a matrix of rows and columns of memory cells (1). To reduce the required memory area a 3T memory cell is proposed comprising a bridge of two bridge transistors (MN0, MN1), preferably NMOS transistors, a read transistor, preferably an PMOS transistor, and a silicided polysilicium fuse resistor (R). The read transistors enable the use of a single sense line (SL) for all memory cells (1) of the same row or column in the matrix thus enabling the use of a common sense amplifier for sensing memory cells (1).

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